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February 15, 2005

09/675578

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: **CERTIFICATE OF CORRECTION**
U. S. Letters Patent No. 6,839,823
Issued: January 4, 2005
For: INCREASED RELIABILITY OF DATA STORED ON FLASH MEMORY IN APPLICATIONS SENSITIVE TO POWER-LOSS
Inventor: See et al.
Our File No. 42390.P4487x

Dear Sir:

Enclosed is the Certificate of Correction (two copies) for the above-referenced patent. Also enclosed is a copy of the original application and corresponding postcard dated September 29, 2000. Please see the previous correction and a copy of the original application indicating that the page number was scanned in.

This request for correction is made under rule 322 of the Rules of Practice and 35 U.S.C. Section 254.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Edwin H. Taylor
Reg. No. 25,129

EHT/jsq
Enclosures

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,839,823

DATED : January 4, 2005

INVENTOR(S) : See et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 3, at line 4, delete "6".

MAILING ADDRESS OF SENDER
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PATENT NO. 6,839,823

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PATENT NO. 6,839,823

Serial/Patent No.: ***** Filing/Issue Date: 9/29/00
Client: INTEL CORPORATION
Title: INCREASED RELIABILITY OF DATA STORED ON FLASH MEMORY IN APPLICATIONS SENSITIVE TO POWER-LOSS
BSTZ File No.: 42390.P4487X Atty/Secty Initials: LJV/MSK/jb
Date Mailed: 9/29/00 Docket Due Date:

The following has been received in the U.S. Patent & Trademark Office on the date stamped hereon:

- ☐ Amendment/Response (____ pgs.)
- ☐ Appeal Brief (____ pgs.) (in triplicate)
- ☒ Application - Utility (34 pgs., with cover and abstract)
- ☐ Application - Rule 1.53(b) Continuation (____ pgs.)
- ☐ Application - Rule 1.53(b) Divisional (____ pgs.)
- ☒ Application - Rule 1.53(b) CIP (34 pgs.)
- ☐ Application - Rule 1.53(d) CPA Transmittal (____ pgs.)
- ☐ Application - Design (____ pgs.)
- ☐ Application - PCT (____ pgs.)
- ☐ Application - Provisional (____ pgs.)
- ☐ Assignment and Cover Sheet
- ☐ Certificate of Mailing
- ☒ Declaration & POA (4 pgs.)
- ☐ Disclosure Docs & Ltr & Copy of Inventor's Signed Letter (____ pgs)
- ☒ Drawings: 23 # of sheets includes 24 figures
- ☒ Express Mail No.: EL672752482US
- ☐ ____ Month(s) Extension of Time
- ☐ Information Disclosure Statement & PTO-1449 (__ pgs.)
- ☐ Issue Fee Transmittal
- ☐ Notice of Appeal
- ☐ Petition for Extension of Time
- ☐ Petition for ____
- ☒ Postcard
- ☐ Power of Attorney (____ pgs.)
- ☐ Preliminary Amendment (____ pgs.)
- ☐ Reply Brief (____ pgs.)
- ☐ Response to Notice of Missing Parts
- ☐ Small Entity Declaration for Indep. Inventor/Small Business
- ☒ Transmittal Letter, in duplicate (2x2 pg.)
- ☒ Fee Transmittal, in duplicate (2x2 pg.)
- ☒ Check No. 37923 Amt: 620.00
- ☐ Check No. ____ Amt: ____

☐ Other: ____

0/11/2000

Due date 12/29/2000 Client Name Intel Corporation

Docket Initial ____ 42390 . P4487X

Dock. Sup. Initial ____

Atty/Initial ____ LJV MSK

Pat/Ser/Reg 675,578 19

Description

month deadline to file prior art disclosure and check related cases based on filed US application).

Attorney's Docket No. 042390.P4487X **PATENT**

UNITED STATES PATENT APPLICATION

FOR

INCREASED RELIABILITY OF DATA STORED ON FLASH MEMORY IN APPLICATIONS SENSITIVE TO POWER-LOSS

Inventors:

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EL672752482US
"Express Mail" mailing label number

9/29/00
Date of Deposit

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

JUANITA BRISCOE
(Typed or printed name of person mailing paper or fee)

(Signature of person mailing paper or fee)

INCREASED RELIABILITY OF DATA STORED ON FLASH MEMORY IN APPLICATIONS SENSITIVE TO POWER-LOSS

CROSS-REFERENCED RELATED APPLICATION

This application is Continuation-in-Part of U.S. Patent Application No. 09/063,954 entitled, "DYNAMIC ALLOCATION FOR EFFICIENT MANAGEMENT OF VARIABLE SIZED DATA WITHIN A NONVOLATILE MEMORY," filed on April 21, 1998.

FIELD OF THE INVENTION

The present relates to computer memory storage systems. More particularly, the present invention relates to dynamic allocation for efficient management of variable sized data within a nonvolatile memory. Specifically, the present relates to increased reliability of data stored on flash memory in applications sensitive to power-loss.

BACKGROUND OF THE INVENTION

Communications devices such as cellular telephones and pagers need the ability to store both data and code. In addition, these communications devices typically require some sort of working memory.

These communication devices generally need to store the code and at least some of the data in nonvolatile memory. For example, serial numbers, authorization codes, frequently dialed numbers, etc. are examples of data that might be stored in nonvolatile memory. Given that the code and data are updated at different frequencies, the communications devices often used different types of nonvolatile memory for storage of data and code. As a result, prior art communications devices typically included one type

of nonvolatile memory for code storage, another nonvolatile memory for data storage, and random access memory such as static random access memory for working memory.

One type of nonvolatile memory is a flash electrically erasable programmable read only memory (flash EEPROM). Flash EEPROM (hereinafter "flash memory") is typically arranged as blocks of single transistor memory cells. Although flash memory is rewritable, the memory cells cannot be re-programmed unless they have first been erased. Moreover, the cells are erasable only in blocks. Thus in order to erase one cell, an entire block of cells must be erased. Updating the flash memory requires some form of media manager to handle copying of valid information out of the block, erasing the block, and writing the valid information as well as the update information to the same or another block. The process of erasing, writing, etc. is relatively time consuming.

Another type of nonvolatile memory is an electrically erasable programmable read only memory (EEPROM) having two-transistor memory cells. Although EEPROM may be arranged into erasable blocks similar to the flash memory, the two-transistor EEPROM is relatively easy to update and does not require the sophisticated media management that flash memory requires for updates. Writing a value to the two-transistor EEPROM cell, however, requires significantly greater time than does programming of an erased single transistor flash memory cell.

One prior art communications device memory architecture includes flash memory for code storage, EEPROM for data storage, and random access memory as working memory.

The use of a variety of nonvolatile memories tends to increase form factor size as well as design and fabrication costs. Personal communications devices such as pagers and cellular telephones are often differentiated based on their size, features, cost, and rate of power consumption.

Moreover as new features are constantly being added, the ratio of code to data may need to change. Providing excess storage for both types of nonvolatile memory increases the cost of the device and is wasteful, unless the storage requirements for both the code and the data are expected to grow. By storing code and data into different types of nonvolatile memory, excess storage capacity in the nonvolatile memory used for code is unavailable for storing data. Similarly, excess storage capacity in the nonvolatile memory used for data is unavailable for storing code. Thus the design is unable to easily accommodate changes in the ratio of nonvolatile memory allocated to code versus that allocated to data.

Furthermore, a common concern with operating a nonvolatile memory device such as a flash memory is power-loss. That is, a sudden loss of power may cause data in the non-volatile memory to be lost or unreliable. Thus, a nonvolatile memory device must be able to recover and to determine the reliability of data in the memory device after a power-loss.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not intended to be limited by the figures of the accompanying drawings, in which like references indicate similar elements and in which:

Figure 1 illustrates storage of code and data in the same monolithic nonvolatile memory device;

Figure 2 illustrates the storage of objects within a block of the nonvolatile memory;

Figure 3 illustrates an object header structure;

Figure 4 illustrates a multiple instance storage structure;

Figure 5 illustrates a sequence table entry and status values;

Figure 6 illustrates the use of a sequence table for identifying the order and location of associated data fragments;

Figure 7 illustrates the use of a group table for identifying the order and location of associated sequence table fragments;

Figure 8 illustrates a method of creating the data lookup table;

Figure 9 illustrates a method of selecting a storage structure in accordance with the size (z) of the data with respect to a plurality of thresholds including: a minimum number of instances (m); an allocation granularity (g); a maximum single instance size ($s*g$); and a maximum sequence table size;

Figure 10 illustrates a method of writing a single instance object;

Figures 11-12 illustrate a method of writing a multiple instance object;

Figures 13-15 illustrate a method of storing an object as a plurality of data fragments;

Figure 16 illustrates a method for appending to a fragmented object when sufficient room is available in the last sequence table fragment;

Figures 17-19 illustrates a method for replacing selected fragments of a fragmented object;

Figure 20 illustrates a method for reclaiming space within the nonvolatile memory;

Figure 21 illustrates a flash memory system;

Figure 22 illustrates a timing diagram for a flash memory system causing storage of invalid data;

Figure 23 illustrates a new data header having redundant power-loss status fields to deal with power-loss; and

Figure 24 illustrates a method for duplicating power-loss status fields.

DETAILED DESCRIPTION

Figure 1 illustrates the storage of both code and data in a monolithic nonvolatile memory device 110. In one embodiment, the nonvolatile memory comprises a plurality of individually erasable blocks. The amount of space allocated to the data and code portions may span one or more blocks as long as the data and code portion do not share a same block.

Nonvolatile memory device 110 has a boot code 112 portion, a data storage 114 portion, a spare block 116, and a code storage 118 portion. The spare block 116 is an actual physical block of the nonvolatile memory device. As will be described below, logical block numbers are used so that the spare block can be any physical block within the data portion 114.

Spare block 116 is used during the reclamation process to recover the valid contents of another block before erasing that other block to free up the space used by invalid contents. Due to the characteristics of flash memory and the relatively long time required to erase a block, superseding data is written to a new location within the nonvolatile memory. The older version of the data is invalidated and the space associated with the invalid data can subsequently be reclaimed by erasing the block after copying any valid data in the block to the spare block. After erasure, the erased block becomes the new spare block.

Figure 2 indicates how data is identified and stored within one of the individual blocks allocated to the data storage 114 portion of Figure 1. The minimal amount of space that can be allocated is referred to as the unit granularity, or simply granularity. The data to be stored is allocated into individual areas spanning one or more units of granularity. Each of these areas is referred to as an object. For example, block 210 includes objects 1, 2, and 3. Each object within the block is identified by an object

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1463-W

P4487X
MTC1

DATE: May 17, 2005
Patent No: 6,839,823
Applicant: See et. al
Issued: 01/04/05

Request for Certificate of Correction:

Consideration has been given your request for the issuance of a certificate of correction for the above-identified patent under the provisions of Rules 1.322.

Respecting the alleged error in column 3,line 4 can not be found. Therefore, no correction(s) is in order here under United States Codes (U.S.C.) 254 Code of Federal Regulation (C.F.R.) 1.322.

In view of the foregoing, your request is hereby denied. A Certificate of Correction will issue for all other matters.

Further consideration will be given upon receipt of a Request for Reconsideration, which should be directed to Decisions and Certificate of Correction Branch. Requests for Reconsideration should be accompanied by additional support (e.g. copy of amendments, post card receipts. PTOL 1449 OR 892,etc.), containing requested data or changes) and /or brief statements of facts, as requested.

RoChaun Johnson for
Cecelia Newman, Supervisor
Decisions and Certificates of Correction
(703) 308-9390 ext. 119

The page # was scanned in.

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